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(54) SEMICONDUCTOR INTEGRATED CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED: To prolong after-shipping service life or to improve after-shipping reliability of a product futher.
SOLUTION: The circuit is provided with an address generating circuit 12 generating an address signal performing in parallel data read-out of memory- macro 1415 for each reset and correction of error detectionM0M1 read-out circuits 1819 performing data read-out of the memory-macro 1415 and correction of error detectionrespectively and outputting a signal indicating correction of error detection and read-out data respectivelycorrection counters 2223 counting signals indicating correction of error detection of the M0M1 read-out circuits 1819 for every reset a comparing circuit 24 inputting count values of the correction counters 2223 for every reset comparing themand outputting a selection signal of the memory-macro corresponding to the minimum count value as a comparison resultand a selector 27 inputting read-out data of the M0M1 read-out circuits 1819 respectivelyselecting them based on the comparison resultand outputting it to a bus.

CLAIMS

[Claim(s)]
[Claim 1]In an integrated circuit provided with two or more memory broad views by which a cell array part of nonvolatile memory with an error-detection-correction function was registered as a macro celland layout wiring was carried outrespectivelyAn integrated circuit calculating the number of times of deed error detection correctionrespectivelycomparing data read and error detection correction of two or more of said memory broad views for every resetrespectivelyand choosing read data of one memory broad view.
[Claim 2]Two or more memory broad views by which a cell array part of nonvolatile memory with an error-detection-correction function was registered as a macro celland

layout wiring was carried outrespectively.
A switch setting circuit which performs switch setting to a product which makes nominal value a partial value of a total memory space value of these memory broad view at the time of a test.
It is the integrated circuit provided with the abovethe number of times of deed error detection correction is calculated for data read and error detection correction of a memory broad view of said plurality for every reset by switch settingrespectivelyit comparesand read data of one memory broad view is chosen.

[Claim 3]The integrated circuit comprising according to claim 1 or 2:
An address generation circuit which generates an address signal which performs data read and error detection correction of two or more of said memory broad views in parallel for every reset.
A decode circuit which decodes said address signal and is outputted to said two or more memory broad viewsrespectively.
Two or more readout circuitries which output a signal and read data in which data read and error detection correction of two or more of said memory broad views are performedrespectivelyand error detection correction is shownrespectively.
Two or more counting circuits which calculate a signal which shows error detection correction of two or more of said readout circuitries for every resetrespectivelyA comparison circuit which inputs enumerated data of two or more of said counting circuitsrespectivelycompares them for every resetand outputs a selection signal of a memory broad view corresponding to the minimum enumerated data as a comparison resultand a selection circuitry which inputs read data of two or more of said readout circuitriesrespectivelyis chosen based on said comparison resultand is outputted to a bus.

[Claim 4]In an integrated circuit provided with two or more memory broad views by which a cell array part of a memory with an error-detection-correction function was registered as a macro celland layout wiring was carried outrespectivelyAn integrated circuit weighting's comparing a situation of deed error detection correction for data read and error detection correction of two or more of said memory broad views for every addressrespectivelyand choosing read data of one memory broad view.
[Claim 5]Two or more memory broad views by which a cell array part of a memory with an error-detection-correction function was registered as a macro celland layout wiring was carried outrespectively.
A switch setting circuit which performs switch setting to a product which makes nominal value a partial value of a total memory space value of these memory broad view at the time of a test.
It is the integrated circuit provided with the aboveand switch setting compares data read and error detection correction of two or more of said memory broad views for every addressweighting compares a situation of deed error detection correctionrespectivelyand read data of one memory broad view is chosen.

[Claim 6]The integrated circuit comprising according to claim 4 or 5:
Two or more readout circuitries which output a signal and read data in which data read and error detection correction of two or more of said memory broad views are

performedrespectivelyand a situation of error detection correction is shownrespectively.
A comparison circuit which inputs a signal which shows a situation of error detection correction of two or more of said readout circuitries for every addressrespectivelycompares by weightingand outputs a selection signal of a memory broad view corresponding to a signal of the minimum dignity as a comparison result.
A selection circuitry which inputs read data of two or more of said readout circuitriesrespectivelyis chosen based on said comparison resultand is outputted to a bus.

[Claim 7]The integrated circuit comprising according to claim 6:
A signal with which a signal which shows a situation of said error detection correction shows error detection.
A signal which shows a correction impossible error.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]Especially this invention relates to the integrated circuit in which switch setting to the product which makes nominal value the partial value of a total memory space value is performed at the time of a test about an integrated circuit.
[0002]
[Description of the Prior Art]Conventionallythis kind of integrated circuit is used in order to develop two or more memory space products by development of one product. For exampledrawing 7 is a block diagram showing the example of this conventional integrated circuit. If drawing 7 is referred tothis conventional integrated circuit will be provided with the address generation circuit 11the decoder 13the memory broad view 14the memory broad view 15the M0 readout circuitry 16the M1 readout circuitry 17the selector 26and the switch setting circuit 27.
[0003]The address generation circuit 11 undergoes outputssuch as a program counterfor examplegenerates the address signal for fetching a program code from the memory broad view 14 or the memory broad view 15outputs it to the decoder 13and outputs an address most significant bit signal to the selector 26.
[0004]The decoder 13 decodes the output from the address generation circuit 12and outputs a decode output to the memory broad view 14 and the memory broad view 15.
[0005]the memory broad view 14 and the memory broad view 15 -- eachConsist of a cell array part of nonvolatile memory with an error-detection-correction functionand the program code for controlling CPU and peripheral equipment is written inWhen reading this program code and the program code which a part of memory broad view broke down and read has an error simultaneouslyin order to carry out error detection correctionan error correction code (ECC) is written in.
[0006]The M0 readout circuitry 16 and the M1 readout circuitry 17 output the program code which performed program code read-out and error detection correction of the memory broad view 14 and the memory broad view 15respectivelyand was read to the selector 26respectively.

[0007]By the logic result of the switch setting signal of the switch setting circuit part 27a macro selection signaland a most significant bit signal in an addressthe selector 26 chooses the output of the M0 readout circuitry 106 or the M1 readout circuitry 109and outputs it to a bus. It is shown in drawing 8 by using the truth value table of the input output function of this selector 26 as an explanatory view.
[0008]The switch setting circuit 27 is performed at the time of the test before shipping the switch setting to the product which makes nominal value the partial value of the total memory space value of the memory broad view 14 and the memory broad view 15 including nonvolatile memory. That isswitch setting of whether both the memory broad view 14 and the memory broad view 15 are used or to use only one of the two is performedand the switch setting signal is outputted to the selector 26.
[0009]Nextthe read operation of the program code in this conventional integrated circuit is explained briefly. Herein order to explain brieflysuppose that the memory space of the two memory broad views 14 and 15 is 128kBrespectively.
[0010]Firstin [when the switch setting signal of the switch setting circuit 27 is "0"] the selector 26As shown in drawing 8the input of a macro selection signal becomes invalid and it corresponds to "0" or "1" in an address of a most significant bit signalThe output of the M0 readout circuitry 16 or the M1 readout circuitry 17 is chosenand the read-out program code of the memory broad view 14 or the memory broad view 15 is outputted to a bus. That isboth the memory broad view 14 and the memory broad view 15 are usedand the nominal value of memory space can be set to 256kB of the memory broad view 14 and memory broad view 15 sum total.
[0011]In [when the switch setting signal of the switch setting circuit 27 is "1" on the other hand] the selector 26As shown in drawing 8the input of a most significant bit signal in an address becomes invalidand it corresponds to "0" or "1" of a macro selection signalThe output of the M0 readout circuitry 16 or the M1 readout circuitry 17 is chosenand the read-out program code of the memory broad view 14 or the memory broad view 15 is outputted to a bus. This macro selection signal as well as the switch setting signal of the switch setting circuit 27When it is determined at the time of the test before product shipment and one of memory broad views are out of order among the memory broad view 14 and the memory broad view 15it is used as a signal for choosing the memory broad view of the side which is not out of order. That isthe output of one of the two of the M0 readout circuitry 16 or the M1 readout circuitry 17 is always chosenone of the two of the memory broad view 14 or the memory broad view 15 is always usedand the nominal value of memory space can be set to 128kB of the memory broad view 14 or the memory broad view 15.
[0012]Thusthe conventional integrated circuit with the switch setting signal of the switch setting circuit 27. or it sets the nominal value of memory space to 256kB of the memory broad view 14 and memory broad view 15 sum total -- one memory -- it is referred to as macroscopic Mino 128kB -- that switch setting is possibletwo or more memory space products can be developed by development of one productand the time and effort of product development can be saved.
[0013]
[Problem(s) to be Solved by the Invention]When only half 128KB which is 256 KB of all the memory space of the memory broad views 14 and 15 in which a program code is written is used in the conventional integrated circuit shown in drawing 7The memory

broad view used after product shipment is being fixedand since the memory broad view read is only memory broad view of one of the twothe life and reliability of the product are limited to the characteristic of one memory broad view. Howeverhigher reliability is searched for in fieldssuch as mount and aerospacenow.
[0014]Thereforethe purpose of this invention is to raise the life cycle or reliability after shipment further.
[0015]
[Means for Solving the Problem]Thereforein an integrated circuit for which this invention is provided with two or more memory broad views by which a cell array part of nonvolatile memory with an error-detection-correction function was registered as a macro celland layout wiring was carried outrespectivelyFor every resetthe number of times of deed error detection correction is calculatedrespectivelydata read and error detection correction of two or more of said memory broad views are comparedand read data of one memory broad view is chosen.
[0016]Two or more memory broad views to which a cell array part of nonvolatile memory with an error-detection-correction function was registered into as a macro celland layout wiring of this invention was carried outrespectivelyIn an integrated circuit provided with a switch setting circuit which performs switch setting to a product which makes nominal value a partial value of a total memory space value of these memory broad view at the time of a testThe number of times of deed error detection correction is calculated for data read and error detection correction of two or more of said memory broad views for every reset by switch settingrespectivelyit comparesand read data of one memory broad view is chosen.
[0017]An address generation circuit which generates an address signal which performs data read and error detection correction of two or more of said memory broad views in parallel for every resetA decode circuit which decodes said address signal and is outputted to said two or more memory broad viewsrespectivelyTwo or more readout circuitries which output a signal and read data in which data read and error detection correction of two or more of said memory broad views are performedrespectivelyand error detection correction is shownrespectivelyTwo or more counting circuits which calculate a signal which shows error detection correction of two or more of said readout circuitries for every resetrespectivelyA comparison circuit which inputs enumerated data of two or more of said counting circuitsrespectivelycompares them for every resetand outputs a selection signal of a memory broad view corresponding to the minimum enumerated data as a comparison resultIt has a selection circuitry which inputs read data of two or more of said readout circuitricsrespectivelyis chosen based on said comparison resultand is outputted to a bus.
[0018]In an integrated circuit for which this invention is provided with two or more memory broad views by which a cell array part of a memory with an error-detection-correction function was registered as a macro celland layout wiring was carried outrespectivelyWeighting compares a situation of deed error detection correction for data read and error detection correction of two or more of said memory broad views for every addressrespectivelyand read data of one memory broad view is chosen.
[0019]Two or more memory broad views to which a cell array part of a memory with an error-detection-correction function was registered into as a macro celland layout wiring of this invention was carried outrespectivelyIn an integrated circuit provided with a

switch setting circuit which performs switch setting to a product which makes nominal value a partial value of a total memory space value of these memory broad view at the time of a testSwitch setting compares data read and error detection correction of two or more of said memory broad views for every addressweighting compares a situation of deed error detection correctionrespectivelyand read data of one memory broad view is chosen.

[0020]Two or more readout circuitries which output a signal and read data in which data read and error detection correction of two or more of said memory broad views are performedrespectivelyand a situation of error detection correction is shownrespectivelyA comparison circuit which inputs a signal which shows a situation of error detection correction of two or more of said readout circuitries for every addressrespectivelycompares by weightingand outputs a selection signal of a memory broad view corresponding to a signal of the minimum dignity as a comparison resultIt has a selection circuitry which inputs read data of two or more of said readout circuitriesrespectivelyis chosen based on said comparison resultand is outputted to a bus.

[0021]A signal which shows a situation of said error detection correction includes a signal which shows error detectionand a signal which shows a correction impossible error.

[0022]

[Embodiment of the Invention]Nextthis invention is explained with reference to drawings. Drawing 1 is a block diagram showing Embodiment 1 of the integrated circuit of this invention. When drawing 1 is referred tothe integrated circuit of this embodimentIt has the address generation circuit 12the decoder 13the memory broad view 14the memory broad view 15the M0 readout circuitry 18the M1 readout circuitry 19the correction counter 22the correction counter 23the comparison circuit 24the selector 26and the switch setting circuit 27. Hereeach block of those other than address generation circuit 12M0 readout circuitry 18M1 readout circuitry 19correction counter 22correction counter 23and comparison circuit 24 is the same as each block of the conventional integrated circuit explained by drawing 7and omits duplication explanation.

[0023]The address generation circuit 12 generates the address signal which performs the data read and error detection correction of each memory broad views 14 and 15 in parallel for every reset corresponding to a reset input signalIt synchronizes with the data read at the time of this resetand the end of error detection correctionOutput a reset output signal to internal CPU etc.and as well as the address generation circuit 11 in drawing 7For exampleoutputssuch as a program counterare undergoneand the address signal for fetching a program code from the memory broad view 14 or the memory broad view 15 is generatedit outputs to the decoder 13and an address most significant bit signal is outputted to the selector 26.

[0024]The M0 readout circuitry 18 and the M1 readout circuitry 19As well as the M0 readout circuitry 16 in drawing 7and the M1 readout circuitry 17Program code read-out and error detection correction of the memory broad view 14 and the memory broad view 15 are performedrespectivelyThe read program code is outputted to the selector 26respectivelyand signal M0ECC and M1ECC which show error detection correction are outputted to the correction counter 22 and the correction counter 23respectively.

[0025]The correction counter 22 and the correction counter 23 correspond to a reset input signalSignal M0ECC and M1ECC which show the error detection correction of the M0 readout circuitry 18 and the M1 readout circuitry 19 for every reset are

calculatedrespectivelyand the enumerated data are outputted to the comparison circuit 24 corresponding to a reset output signalrespectively.
[0026]For every resetthe comparison circuit 24 inputs the enumerated data of the correction counter 22 and the correction counter 23respectivelycompares themand outputs them to the selector 26 synchronizing with "1" change of a reset output signal by making the selection signal of the memory broad view corresponding to the minimum enumerated data into a comparison result. For examplewhen the enumerated data of the correction counter 23 are smaller than the enumerated data of the correction counter 22a comparison result "1" is outputted to the selector 26.
[0027]Drawing 2 is a timing diagram showing the example of read operation in the integrated circuit of this embodiment. With reference to drawing 8 and drawing 2the read operation in the integrated circuit of this embodiment is explained. Herein order to explain simplememory space of the memory broad view 14 and the memory broad view 15 is set to 128kB as well as the formerrespectively.
[0028]Firstwhen the switch setting signal of the switch setting circuit 27 is "0"in the selector 26the comparison result of the comparison circuit 24 is inputted as a macro selection signalbut. As shown in drawing 8the input of a macro selection signal becomes invalid and it corresponds to "0" or "1" in an address of a most significant bit signalThe output of the M0 readout circuitry 18 or the M1 readout circuitry 19 is chosenand the read-out program code of the memory broad view 14 or the memory broad view 15 is outputted to a bus. That isboth the memory broad view 14 and the memory broad view 15 are usedand the nominal value of memory space can be set to 256kB of the memory broad view 14 and memory broad view 15 sum total.
[0029]On the other handwhen the switch setting signal of the switch setting circuit 27 is "1"memory space to be used is set to 128kBand the program code of the identical content is beforehand written in the memory broad view 104 and the memory broad view 107. In the selector 26as shown in drawing 8the input of a most significant bit signal in an address becomes invalidand it corresponds to "0" or "1" of a comparison result inputted as a macro selection signal[of the comparison circuit 24] The output of the M0 readout circuitry 18 or the M1 readout circuitry 19 is chosenand the read-out program code of the memory broad view 14 or the memory broad view 15 is outputted to a bus.
[0030]The comparison result of this comparison circuit 24 is outputted by the result of the data read of each memory broad views 14 and 15 and error detection correction which are performed in parallel for every reset by the timing T0 - Tn-1 synchronizing with "1" change of the reset output signal of the timing Tnas shown in drawing 2.
[0031]Firstin the timing T0power supply voltage is switched ona reset input signal is set to "0"the address generation circuit 12the M0 readout circuitry 18the M1 readout circuitry 19the correction counter 22and the correction counter 23 are resetand a comparison result is set to "0."
[0032]Thena reset input signal is set to "1" in the timing T1During the period when the address generation circuit 12 is outputting "0" as a reset output signalThe address signal of the address value which **********ed one by one from the lowest address to the highest address to the memory broad view 14 and the memory broad view 15 is generatedThe program code and error correction code ECC of the address specified by the decoder 13 are read from the memory broad view 14 and the memory broad view 15 in parallel with the M0 readout circuitry 18 and the M1 readout circuitry 19.

[0033]In the timing T2since correction by error correction code ECC was performed to the program code read from the memory broad view 14signal M0ECC which shows error detection correction is set to "1"and the correction counter 22 counts up and it becomes enumerated data of 1 h in the M0 readout circuitry 18. In the M1 readout circuitry 19since correction by error correction code ECC is not performed to the program code read from the memory broad view 107signal M1ECC which shows error detection correction is "0"and the correction counter 23 is not counted up but is still enumerated data of 0 h.

[0034]In timing T3like the timing T2in the M0 readout circuitry 18. Since correction by error correction code ECC was performed to the program code read from the memory broad view 14signal M0ECC is set to "1"and the correction counter 22 is counted up and becomes enumerated data of 2 h. In the M1 readout circuitry 19since correction by error correction code ECC is not performed to the program code read from the memory broad view 15signal M1ECC does not count up the correction counter 23 with "0"but is still enumerated data of 0 h.

[0035]In the timing T4in the M0 readout circuitry 18since correction by error correction code ECC is not performed to the program code read from the memory broad view 14signal M0ECC does not count up the correction counter 22 with "0"but is still enumerated data of 2 h. In the M1 readout circuitry 19since correction by error correction code ECC was performed to the program code read from the memory broad view 15signal M1ECC is set to "1"and the correction counter 207 is counted up and becomes enumerated data of 1 h.

[0036]In timing Tn-2like timing T3since correction by error correction code ECC was performedthe correction counter 22 is counted up and becomes enumerated data of 3 h in the M0 readout circuitry 18. In the M1 readout circuitry 19since correction by error correction code ECC is not performedthe correction counter 23 is not counted up but is still enumerated data of 1 h.

[0037]In timing Tn-1** and the correction counter 22 with which it is the M0 readout circuitry 18and correction by error correction code ECC is not performed like the timing T4 are not counted upbut are still enumerated data of 3 h. In the M1 readout circuitry 19since correction by error correction code ECC was performedthe correction counter 23 is counted up and becomes enumerated data of 2 h.

[0038]Nextin the timing Tnthe address signal outputted from the address generation circuit 12 changes from the highest address of a memory broad view to the lowest addressand a reset output signal changes to "1." Synchronizing with "1" change of this reset output signalthe comparison circuit 24 compares the enumerated data of the both sides of the correction counter 22 and the correction counter 23and in this casesince the enumerated data of the correction counter 23 are smaller than the enumerated data of the correction counter 221is outputted to a comparison result. It always becomes an output of the M1 readout circuitry 17the program code of the memory broad view 15 is outputted to a busand the output of the selector 26 which inputs this comparison result "1" as a macro selection signal is fetched by CPUas shown in drawing 8.

[0039]After a reset output signal is set to 1the address generation circuit 201Outputssuch as a program counterare undergonethe address signal for fetching a program code from the memory broad view 14 or the memory broad view 15 is generatedthe program code of the memory broad view 15 is outputted to a bus by the selector 26and CPU fetches.

[0040]Although the comparison result was set to 1 and the program code of the memory broad view 15 took up the example outputted to a bus in explanation of the timing diagram of drawing 2 of operation synchronizing with "1" change of a reset output signalThe enumerated data of the correction counter 22 are the same as that of the correction counter 23or when smaller than ita comparison result is set to "0"and the program code of the memory broad view 14 is outputted to a busand is fetched by CPU.
[0041]As mentioned abovein the integrated circuit of this embodiment. For every resetthe error detection correction of the memory broad views 14 and 15 can be calculatedrespectivelyand can be comparedthe small memory broad view of enumerated data can be chosena memory broad view with the sufficient characteristic can be usedthere is almost no increase in a chip sizeand the life cycle and reliability after shipment can be extended.
[0042]For examplethe example which sets composition of a memory broad view to 1 block =32 bit+ECC6bitand performs 1-bit correction is explained below. Drawing 3 is the explanatory view in which the effect in this example was summarized.
[0043]Per blockthe poor probability FB will be called for by the following formulaif an average defective fraction is set to P per bit.
$FB=1-\{(1-P)^{38}+38*P(1-P)^{37}\}$ (unit: ppm)
Temporarilyper bit of the memory broad view 14 in early stages of a productif the defective fraction P shall be 0.25 ppm per bit of 0.2 ppm and the memory broad view 15the defective fraction PThe poor probability FB is set to 0.000028 ppm and 0.000044 ppm per block of the memory broad view 14 and the memory broad view 15respectively.
[0044]Nextpoor probability FM of the memory broad view of 128kB is converted from the inferior-goods probability FB per blockand is calculated by the following formula.
$FM=1-(1-FB)^{32768}$ (unit: ppm)
If this formula is applied to the memory broad view 14 in early stages of a productand the memory broad view 15memory macroscopic per poor probability FM of the memory broad view 14 and the memory broad view 15 will be set to 0.92 ppm and 1.44 ppmrespectively.
[0045]Nextif it assumes that the defective fraction P fell to 0.4 ppm per bit of the memory broad view 14 ten years afterwardand the defective fraction P fell to 0.3 ppm per bit of the memory broad view 107Memory macroscopic per poor probability FM of the memory broad view 14 and the memory broad view 15 is set to 3.69 ppm and 2.07 ppm from an above-mentioned formularespectively.
[0046]For this reasonin the conventional integrated circuitsince the memory broad view 14 with low poor probability is chosen and fixed at the time of the test before the early-stagesi.e.productshipment of a productthe inferior-goods probability as a product is set to 3.69 ppm. On the other handin the integrated circuit of this embodimentsince the memory broad view 15 with low poor probability is chosen in ten yearsthe inferior-goods probability as a product is set to 2.07 ppmand will improve only by 1.62 ppm from the conventional integrated circuit ten years after product shipment.
[0047]Drawing 4 is a block diagram showing Embodiment 2 of the integrated circuit of this invention. If drawing 4 is referred tothe integrated circuit of this embodiment will be provided with the address generation circuit 11the decoder 13the memory broad view 14the memory broad view 15the M0 readout circuitry 20the M1 readout circuitry 21the comparison circuit 25the selector 26and the switch setting circuit 27. Hereeach block of

those other than M0 readout circuitry 20M1 readout circuitry 21and comparison circuit 25 is the same as each block of the conventional integrated circuit explained by drawing 7and omits duplication explanation.
[0048]The M0 readout circuitry 20 and the M1 readout circuitry 21As well as the M0 readout circuitry 16 in drawing 7and the M1 readout circuitry 17Program code read-out and error detection correction of the memory broad view 14 and the memory broad view 15 are performedrespectivelythe read program code is outputted to the selector 26respectivelyand the signal which shows the situation of error detection correction is outputted to the comparison circuit 25respectively. The signal which shows the situation of these error detection correctionincluding two signals respectively the M0 readout circuitry 20Outputting signal M0ECC which shows error detectionand signal M0ERR which shows a correction impossible errorthe M1 readout circuitry 21 outputs signal M1ECC which shows a correction impossible errorand signal M1ERR which shows a correction impossible error.
[0049]Namelysignal M0ECC and M0ERR which show the situation of error detection correctionWhen error detection is not carried out to the program code read from the memory broad view 14it is set to "0" and "0"respectivelywhen an error correction is carried outit is set to "1" and "0"respectivelyand when an error correction is impossibleit is set to "1" and "1"respectively. Signal M1ECC which shows the situation of error detection correctionand M1ERR are similarly outputted to the program code read from the memory broad view 15.
[0050]The comparison circuit 25 inputs signal M0ECCM0ERR and signal M1ECCand M1ERR from the M0 readout circuitry 20 and the M1 readout circuitry 21 for every addressrespectivelyWeighting is carried out to signal M0ECC or M1ECC< signal M0ERR or M1ERRand it comparesand outputs to the selector 26 by making the selection signal of the memory broad view corresponding to the signal of small dignity into a comparison result. For exampleif it is signal M0ECCM0ERR<= signal M1ECCand M1ERRa comparison result "0" will be outputted to the selector 26and if it is signal M0ECCM0ERR> signal M1ECCand M1ERRa comparison result "1" will be outputted to the selector 26.
[0051]Drawing 5 is a timing diagram showing the example of read operation in the integrated circuit of this embodiment. With reference to drawing 8 and drawing 5the read operation in the integrated circuit of this embodiment is explained. Herein order to explain simplememory space of the memory broad view 14 and the memory broad view 15 is set to 128kB as well as the formerrespectively.
[0052]Firstwhen the switch setting signal of the switch setting circuit 27 is "0"in the selector 26the comparison result of the comparison circuit 25 is inputted as a macro selection signalbut. As shown in drawing 8the input of a macro selection signal becomes invalid and it corresponds to "0" or "1" in an address of a most significant bit signalThe output of the M0 readout circuitry 20 or the M1 readout circuitry 21 is chosenand the read-out program code of the memory broad view 14 or the memory broad view 15 is outputted to a bus. That isboth the memory broad view 14 and the memory broad view 15 are usedand the nominal value of memory space can be set to 256kB of the memory broad view 14 and memory broad view 15 sum total.
[0053]On the other handwhen the switch setting signal of the switch setting circuit 27 is "1"memory space to be used is set to 128kBand the program code of the identical content

is beforehand written in the memory broad view 104 and the memory broad view 107. In the selector 26as shown in drawing 8the input of a most significant bit signal in an address becomes invalidand it corresponds to "0" or "1" of a comparison result inputted as a macro selection signal[of the comparison circuit 25] The output of the M0 readout circuitry 20 or the M1 readout circuitry 21 is chosenand the read-out program code of the memory broad view 14 or the memory broad view 15 is outputted to a bus.
[0054]The comparison result of this comparison circuit 25 is outputted by the result of the data read of each memory broad views 14 and 15 and error detection correction which are performed in parallel for every address to the timing T0-T9 as shown in drawing 5.
[0055]Firstin the timing T0power supply voltage is switched ona reset input signal is set to "0"the address generation circuit 11the M0 readout circuitry 20the M1 readout circuitry 21and the comparison circuit 25 are resetand a comparison result is set to "0."
[0056]Thena reset input signal is set to "1" after the timing T1Reset is canceled and the address generation circuit 12 undergoes outputssuch as a program counterfor exampleGenerate the address 0the address a - the address g in order as an address signal for fetching a program code from the memory broad view 14 or the memory broad view 15and it outputs to the decoder 13The program code and error correction code ECC of the same address specified by the decoder 13 are read from the memory broad view 14 and the memory broad view 15 in parallel with the M0 readout circuitry 20 and the M1 readout circuitry 21.
[0057]In the M0 readout circuitry 20 and the M1 readout circuitry 21program code read-out and error detection correction of the memory broad view 14 and the memory broad view 15 are performedrespectivelyThe read program code is outputted to the selector 26respectivelyand the signal which shows the situation of error detection correction is outputted to the comparison circuit 25respectivelyFrom the comparison circuit 25it is outputted to the selector 26 as a macro selection signal by the comparison result for every addressand by the selector 26. The output of the M0 readout circuitry 20 or the M1 readout circuitry 21 is chosen for every addressand the program code of the memory broad view 14 or the memory broad view 15 is outputted to a busand is fetched by CPU.
[0058]For examplesince the program code of the address a of the memory broad view 14 and the memory broad view 15 did not have the necessity for correction of both sides in the timing T2Signal M0ECC which shows the situation of error detection correctionM0ERR and signal M1ECCand M1ERR are set to "00"and "00"a comparison result is set to "0"and the program code of the memory broad view 14 is outputted to a bus.
[0059]In timing T3although the program code of the address b of the memory broad view 14 did not have the necessity for correction on the memory broad view 14Since restoration according [the program code of the address b of the memory broad view 15] to correction was performedsignal M0ECCM0ERR and signal M1ECCand M1ERR are set to "00"and "10"a comparison result is set to "0"and the program code of the memory broad view 14 is outputted to a bus.
[0060]In the timing T4although restoration by correction was performedthe program code of the address c of the memory broad view 14Since the program code of the address c of the memory broad view 15 did not have the necessity for correctionsignal M0ECCM0ERR and signal M1ECCand M1ERR are set to "10"and "00"a comparison result is set to "1"and the program code of the memory broad view 15 is outputted to a

bus.
[0061]In the timing T5although restoration by correction was performedthe program code of the address d of the memory broad view 14Since it was unrestorablethe program code of the address d of the memory broad view 15 also by correction signal M0ECCM0ERR and signal M1ECCand M1ERRIt is set to "10"and "11"a comparison result is set to "0"and the program code of the memory broad view 14 is outputted to a bus.
[0062]In the timing T6although the program code of the address e of the memory broad view 14 was unrestorable also by correctionSince restoration according [the program code of the address e of the memory broad view 15] to correction was performedsignal M0ECCM0ERR and signal M1ECCand M1ERR are set to "11"and "10"a comparison result is set to "1"and the program code of the memory broad view 15 is outputted to a bus.
[0063]In the timing T7although the program code of the address f of the memory broad view 14 did not have the necessity for correctionSince it was unrestorablethe program code of the address f of the memory broad view 15 also by correction signal M0ECCM0ERR and signal M1ECCand M1ERRIt is set to "00"and "11"a comparison result is set to "0"and the program code of the memory broad view 14 is outputted to a bus.
[0064]In the timing T8although the program code of the address g of the memory broad view 14 was unrestorable also by correctionSince the program code of the address g of the memory broad view 15 did not have the necessity for correctionsignal M0ECCM0ERR and signal M1ECCand M1ERR are set to "11"and "00"a comparison result is set to "1"and the program code of the memory broad view 15 is outputted to a bus.
[0065]Since restoration according [the program code of the address h of the memory broad view 14] to correction was performed and restoration also according [the program code of the address h of the memory broad view 15] to correction was performed in the timing T9Signal M0ECCM0ERR and signal M1ECCand M1ERR are set to "10"and "10"a comparison result is set to "0"and the program code of the memory broad view 14 is outputted to a bus.
[0066]As mentioned abovesince restoration by correction can choose few memory broad views for every single address of a memory broad viewwith the integrated circuit of this embodimentthe life cycle and reliability after shipment can be extended further.
[0067]For examplethe example which sets composition of a memory broad view to 1 block =32 bit+ECC6bitand performs 1-bit correction is explained below. Drawing 6 is the explanatory view in which the effect in this example was summarized.
[0068]The percentages which are the defective fractions per bit of P= 0.20 ppm in the memory broad view 14 and the memory broad view 15 are 70% and 50% temporarilyrespectivelyWhen the percentages which are the defective fractions per bit of P= 0.25 ppm are 30% and 50%respectivelyper bit of the memory broad view 14 and the memory broad view 15 the average defective fraction P. It is set to 0.22 ppm and 0.23 ppmrespectivelyand memory macroscopic per poor probability FM of the memory broad view 14 and the memory broad view 15 is set to 1.06 ppm and 1.17 ppm by the above-mentioned formularespectively. In the conventional integrated circuit shown in drawing 7since the low memory broad view of poor probability FM is chosenthe memory broad view 14 is chosen and the inferior-goods probability as a product is set to 1.06 ppm.

[0069]On the other handin the integrated circuit of this embodimentin order to explain brieflythe defective fraction P per bit on the memory broad view 14 the memory broad view 15 of the same address as a high addressThe defective fraction P per bit assumes that it is lowandin the defective fraction Pthe defective fraction P assumes altogether the memory broad view 14 of the same address as a high address to be low per bit per bit on the memory broad view 15 conversely. Per bit of the address of the memory broad view chosen by the selector 26 in such a casethe defective fraction P is altogether set to 0.2 ppmand the inferior-goods probability as a product is set to 0.92 ppmand improves only by 0.14 ppm from the conventional integrated circuit.
[0070]Although the integrated circuit of Embodiments 1 and 2 mentioned above has explained the case where two or more memory space products are developed by development of one productby the switch setting of whether the nominal value of memory space is considered as the sum total of two memory broad viewsor to consider it only as one memory broad viewIt is also possible to consider it as the integrated circuit for high-reliability which is not provided with a switch setting circuit from the startbut uses only the one-copy memory space of the memory space sum total of two or more memory broad view.
[0071]
[Effect of the Invention]As explained abovethe integrated circuit by this invention does not almost have the increase in a chip sizeand there is an effect of the life cycle and reliability after shipment improving.
[0072]The reason is because the error detection correction of each memory broad view can be calculatedrespectivelyand can be compared for every resetthe small memory broad view of enumerated data can be chosen and a memory broad view with the sufficient characteristic can be used. It is because restoration by correction can choose few memory broad views for every single address of a memory broad view.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a block diagram showing Embodiment 1 of the integrated circuit of this invention.
[Drawing 2]It is a timing diagram showing the example of read operation in the integrated circuit of drawing 1.
[Drawing 3]It is an explanatory view for explaining the effect of the integrated circuit of drawing 1.
[Drawing 4]It is a block diagram showing Embodiment 2 of the integrated circuit of this invention.
[Drawing 5]It is a timing diagram showing the example of read operation in the integrated circuit of drawing 4.
[Drawing 6]It is an explanatory view for explaining the effect of the integrated circuit of drawing 4.
[Drawing 7]It is a block diagram showing one example of the conventional integrated circuit.
[Drawing 8]It is an explanatory view showing the truth value table of the input output

function of the selector 26 in the integrated circuit of drawing 7.
[Description of Notations]
1112 address generation circuits
13 Decoder
14 and 15 Memory broad view
161820 M0 readout circuitry
171921 M1 readout circuitry
22 and 23 Correction counter
24 and 25 Comparison circuit
26 Selector
27 Switch setting circuit